

# SN65C1167, SN75C1167, SN65C1168, SN75C1168 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

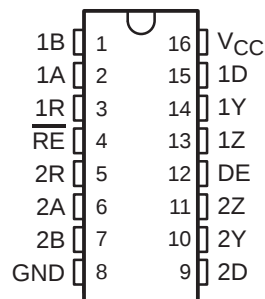
SLLS159E – MARCH 1993 – REVISED NOVEMBER 2003

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- BiCMOS Process Technology
- Low Supply-Current Requirements:  
9 mA Max
- Low Pulse Skew
- Receiver Input Impedance . . . 17 k $\Omega$  Typ
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Common-Mode Input Voltage Range of -7 V to 7 V
- Operate From Single 5-V Power Supply
- Glitch-Free Power-Up/Power-Down Protection
- Receiver 3-State Outputs Active-Low Enable for SN65C1167 and SN75C1167 Only
- Improved Replacements for the MC34050 and MC34051

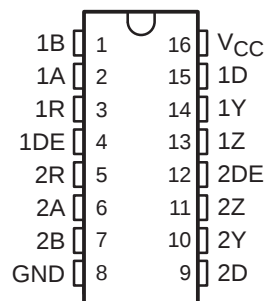
## description/ordering information

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

SN65C1167 . . . DB OR NS PACKAGE  
SN75C1167 . . . DB, N, OR NS PACKAGE  
(TOP VIEW)



SN65C1168 . . . N, NS, OR PW PACKAGE  
SN75C1168 . . . DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP (N)   | Tube          | SN75C1167N            | SN75C1167N       |
|                | SOP (NS)   | Tape and reel | SN75C1167NSR          | 75C1167          |
|                | SSOP (DB)  | Tape and reel | SN75C1167DBR          | CA1167           |
|                | PDIP (N)   | Tube          | SN75C1168N            | SN75C1168N       |
|                | SOP (NS)   | Tape and reel | SN75C1168NSR          | 75C1168          |
|                | SSOP (DB)  | Tape and reel | SN75C1168DBR          | CA1168           |
|                | TSSOP (PW) | Tube          | SN75C1168PW           | CA1168           |
|                |            | Tape and reel | SN75C1168PWR          |                  |
| -40°C to 85°C  | SOP (NS)   | Tape and reel | SN65C1167NSR          | 65C1167          |
|                | SSOP (DB)  | Tape and reel | SN65C1167DBR          | CB1167           |
|                | PDIP (N)   | Tube          | SN65C1168N            | SN65C1168N       |
|                | SOP (NS)   | Tape and reel | SN65C1168NSR          | 65C1168          |
|                | TSSOP (PW) | Tube          | SN65C1168PW           | CB1168           |
|                |            | Tape and reel | SN65C1168PWR          |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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# SN65C1167, SN75C1167, SN65C1168, SN75C1168

## DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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### description/ordering information (continued)

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

### Function Tables

EACH DRIVER

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | Y       | Z |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |

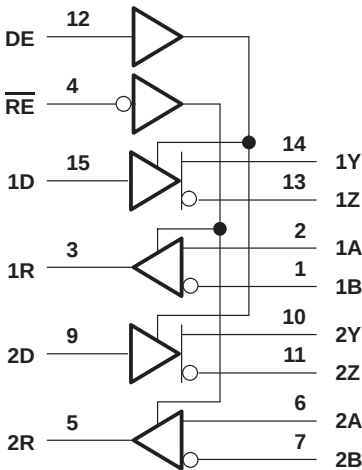
SN75C1167, EACH RECEIVER

| DIFFERENTIAL INPUTS<br>A – B            | ENABLE<br>RE | OUTPUT<br>R |
|-----------------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2\text{ V}$              | L            | H           |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2\text{ V}$             | L            | L           |
| X                                       | H            | Z           |
| Open                                    | L            | H           |

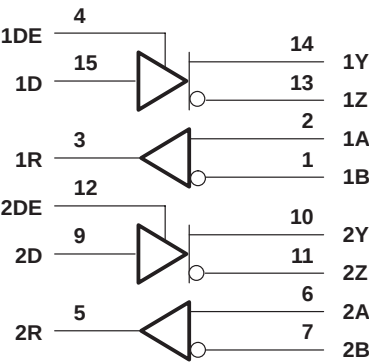
H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

### logic diagram (positive logic)

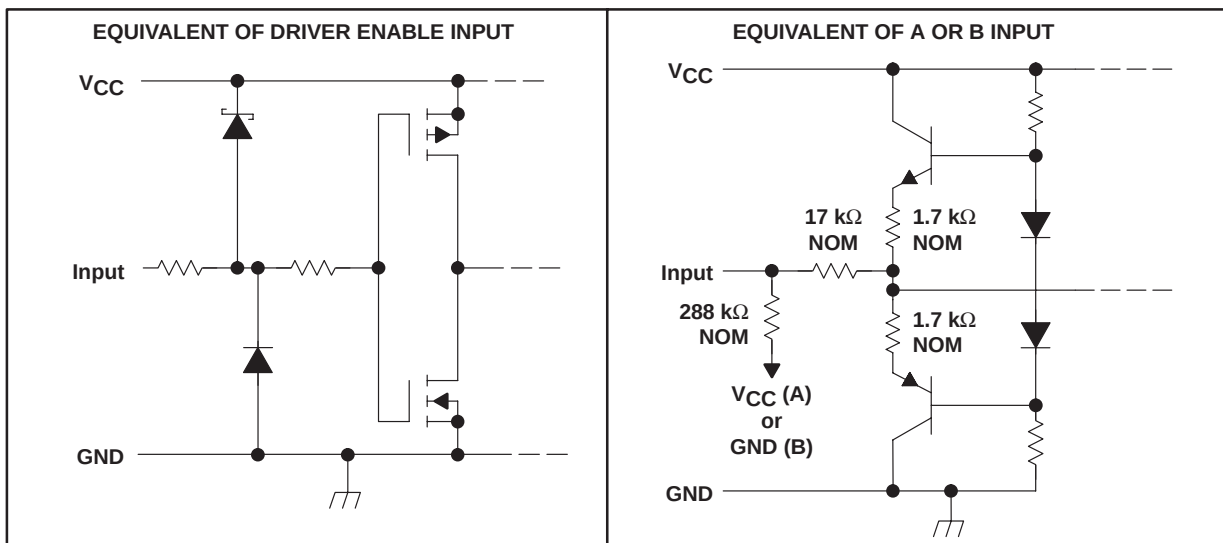
SN65C1167/SN75C1167



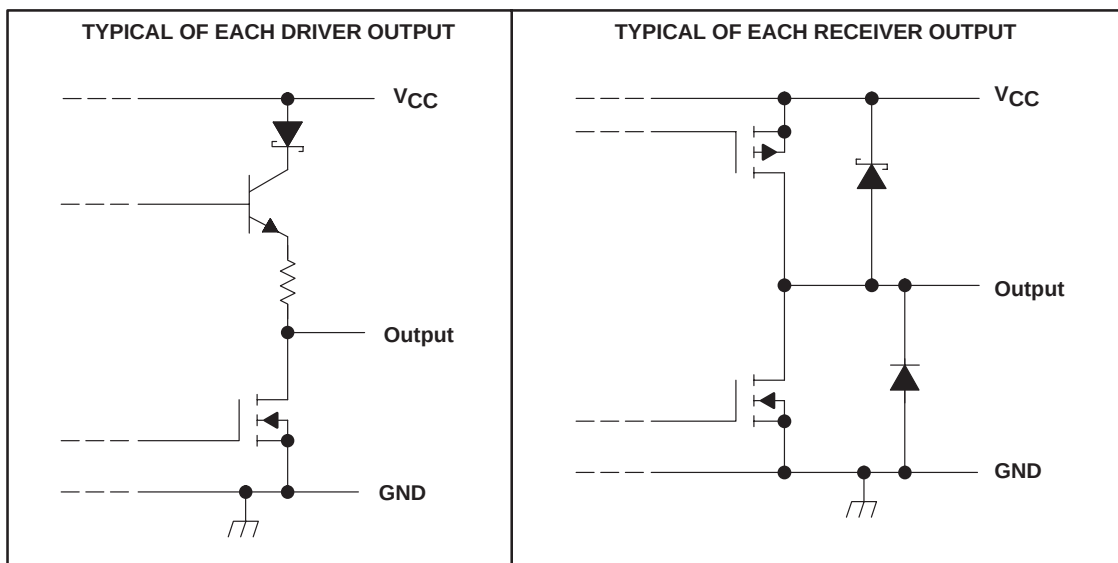
SN65C1168, SN75C1168



## schematics of inputs



## schematics of outputs



# SN65C1167, SN75C1167, SN65C1168, SN75C1168

## DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                          |                            |
|--------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)                              | –0.5 V to 7 V              |
| Input voltage range, $V_I$                                               | –0.5 V to $V_{CC} + 0.5$ V |
| Input voltage range, $V_I$ (A or B, Receiver)                            | –11 V to 14 V              |
| Differential input voltage range, $V_{ID}$ , Receiver (see Note 2)       | –14 V to 14 V              |
| Output voltage range, $V_O$ , Driver                                     | –5 V to 7 V                |
| Clamp current range, $I_{IK}$ or $I_{OK}$ , Driver                       | ±20 mA                     |
| Output current range, $I_O$ , Driver                                     | ±150 mA                    |
| Supply current, $I_{CC}$                                                 | 200 mA                     |
| GND current                                                              | –200 mA                    |
| Output current range, $I_O$ , Receiver                                   | ±25 mA                     |
| Operating virtual junction temperature                                   | 150°C                      |
| Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): DB package | 82°C/W                     |
| N package                                                                | 67°C/W                     |
| NS package                                                               | 64°C/W                     |
| PW package                                                               | 108°C/W                    |
| Storage temperature range, $T_{stg}$                                     | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values except differential input voltage are with respect to the network GND.  
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.  
3. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.  
4. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

|          |                                        |                      | MIN | NOM | MAX | UNIT |
|----------|----------------------------------------|----------------------|-----|-----|-----|------|
| $V_{CC}$ | Supply voltage                         |                      | 4.5 | 5   | 5.5 | V    |
| $V_{IC}$ | Common-mode input voltage (see Note 5) | Receiver             |     |     | ±7  | V    |
| $V_{ID}$ | Differential input voltage             | Receiver             |     |     | ±7  | V    |
| $V_{IH}$ | High-level input voltage               | Except A, B          | 2   |     |     | V    |
| $V_{IL}$ | Low-level input voltage                | Except A, B          |     |     | 0.8 | V    |
| $I_{OH}$ | High-level output current              | Receiver             |     |     | –6  | mA   |
|          |                                        | Driver               |     |     | –20 |      |
| $I_{OL}$ | Low-level output current               | Receiver             |     |     | 6   | mA   |
|          |                                        | Driver               |     |     | 20  |      |
| $T_A$    | Operating free-air temperature         | SN75C1167, SN75C1168 | 0   |     | 70  | °C   |
|          |                                        | SN65C1167, SN65C1168 | –40 |     | 85  |      |

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.



# SN65C1167, SN75C1167, SN65C1168, SN75C1168 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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## DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| PARAMETER                                                              | TEST CONDITIONS                                                          | MIN                                       | TYP <sup>†</sup> | MAX  | UNIT |
|------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------|------------------|------|------|
| V <sub>IK</sub> Input clamp voltage                                    | I <sub>I</sub> = -18 mA                                                  |                                           |                  | -1.5 | V    |
| V <sub>OH</sub> High-level output voltage                              | V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -20 mA | 2.4                                       | 3.4              |      | V    |
| V <sub>OL</sub> Low-level output voltage                               | V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA  |                                           | 0.2              | 0.4  | V    |
| V <sub>OD1</sub>   Differential output voltage                         | I <sub>O</sub> = 0 mA                                                    | 2                                         |                  | 6    | V    |
| V <sub>OD2</sub>   Differential output voltage                         | R <sub>L</sub> = 100 Ω, See Figure 1 and Note 5                          | 2                                         | 3.1              |      | V    |
| Δ V <sub>OD</sub>   Change in magnitude of differential output voltage |                                                                          |                                           |                  | ±0.4 | V    |
| V <sub>OC</sub> Common-mode output voltage                             |                                                                          |                                           |                  | ±3   | V    |
| Δ V <sub>OC</sub>   Change in magnitude of common-mode output voltage  |                                                                          |                                           |                  | ±0.4 | V    |
| I <sub>O(OFF)</sub> Output current with power off (see Note 3)         | V <sub>CC</sub> = 0 V                                                    | V <sub>O</sub> = 6 V                      |                  | 100  | μA   |
|                                                                        |                                                                          | V <sub>O</sub> = -0.25 V                  |                  | -100 | μA   |
| I <sub>OZ</sub> High-impedance-state output current                    | V <sub>O</sub> = 2.5 V                                                   |                                           |                  | 20   | μA   |
|                                                                        | V <sub>O</sub> = 5 V                                                     |                                           |                  | -20  |      |
| I <sub>IH</sub> High-level input current                               | V <sub>I</sub> = V <sub>CC</sub> or V <sub>IH</sub>                      |                                           |                  | 1    | μA   |
| I <sub>IL</sub> Low-level input current                                | V <sub>I</sub> = GND or V <sub>IL</sub>                                  |                                           |                  | -1   | μA   |
| I <sub>OS</sub> Short-circuit output current                           | V <sub>O</sub> = V <sub>CC</sub> or GND, See Note 6                      |                                           | -30              | -150 | mA   |
| I <sub>CC</sub> Supply current (total package)                         | No load, Enabled                                                         | V <sub>I</sub> = V <sub>CC</sub> or GND   |                  | 4    | mA   |
|                                                                        |                                                                          | V <sub>I</sub> = 2.4 or 0.5 V, See Note 7 |                  | 5    |      |
| C <sub>i</sub> Input capacitance                                       |                                                                          |                                           | 6                |      | pF   |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

NOTES: 5. Refer to TIA/EIA-422-B for exact conditions.

6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7. This parameter is measured per input, while the other inputs are at V<sub>CC</sub> or GND.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| PARAMETER                                                          | TEST CONDITIONS                                                                                                                                            | MIN | TYP <sup>†</sup> | MAX | UNIT |
|--------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------------------|-----|------|
| t <sub>PHL</sub> Propagation delay time, high- to low-level output | R <sub>1</sub> = R <sub>2</sub> = 50 Ω, R <sub>3</sub> = 500 Ω,<br>C <sub>1</sub> = C <sub>2</sub> = C <sub>3</sub> = 40 pF, S1 is open,<br>See Figure 2   |     | 7                | 12  | ns   |
| t <sub>PLH</sub> Propagation delay time, low- to high-level output |                                                                                                                                                            |     | 7                | 12  | ns   |
| t <sub>sk(p)</sub> Pulse skew                                      |                                                                                                                                                            |     | 0.5              | 4   | ns   |
| t <sub>r</sub> Rise time                                           | R <sub>1</sub> = R <sub>2</sub> = 50 Ω, R <sub>3</sub> = 500 Ω,<br>C <sub>1</sub> = C <sub>2</sub> = C <sub>3</sub> = 40 pF, S1 is open,<br>See Figure 3   |     | 5                | 10  | ns   |
| t <sub>f</sub> Fall time                                           |                                                                                                                                                            |     | 5                | 10  | ns   |
| t <sub>PZH</sub> Output enable time to high level                  | R <sub>1</sub> = R <sub>2</sub> = 50 Ω, R <sub>3</sub> = 500 Ω,<br>C <sub>1</sub> = C <sub>2</sub> = C <sub>3</sub> = 40 pF, S1 is closed,<br>See Figure 4 |     | 10               | 19  | ns   |
| t <sub>PZL</sub> Output enable time to low level                   |                                                                                                                                                            |     | 10               | 19  | ns   |
| t <sub>PHZ</sub> Output disable time from low level                | R <sub>1</sub> = R <sub>2</sub> = 50 Ω, R <sub>3</sub> = 500 Ω,<br>C <sub>1</sub> = C <sub>2</sub> = C <sub>3</sub> = 40 pF, S1 is closed,<br>See Figure 4 |     | 7                | 16  | ns   |
| t <sub>PLZ</sub> Output disable time from high level               |                                                                                                                                                            |     | 7                | 16  | ns   |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.



# SN65C1167, SN75C1167, SN65C1168, SN75C1168

## DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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### RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

| PARAMETER |                                                            | TEST CONDITIONS                            | MIN                                   | TYP <sup>†</sup> | MAX     | UNIT       |
|-----------|------------------------------------------------------------|--------------------------------------------|---------------------------------------|------------------|---------|------------|
| $V_{IT+}$ | Positive-going input threshold voltage, differential input |                                            |                                       |                  | 0.2     | V          |
| $V_{IT-}$ | Negative-going input threshold voltage, differential input |                                            | -0.2 <sup>‡</sup>                     |                  |         | V          |
| $V_{hys}$ | Input hysteresis ( $V_{IT+} - V_{IT-}$ )                   |                                            |                                       | 60               |         | mV         |
| $V_{IK}$  | Input clamp voltage, $\overline{RE}$                       | SN75C1167<br>$I_I = -18$ mA                |                                       |                  | -1.5    | V          |
| $V_{OH}$  | High-level output voltage                                  | $V_{ID} = 200$ mV, $I_{OH} = -6$ mA        | 3.8                                   | 4.2              |         | V          |
| $V_{OL}$  | Low-level output voltage                                   | $V_{ID} = -200$ mV, $I_{OL} = 6$ mA        |                                       | 0.1              | 0.3     | V          |
| $I_{OZ}$  | High-impedance-state output current                        | SN75C1167<br>$V_O = V_{CC}$ or GND         |                                       | $\pm 0.5$        | $\pm 5$ | $\mu$ A    |
| $I_I$     | Line input current                                         | Other input at 0 V                         | $V_I = 10$ V                          |                  | 1.5     | mA         |
|           |                                                            |                                            | $V_I = -10$ V                         |                  | -2.5    |            |
| $I_I$     | Enable input current, $\overline{RE}$                      | SN75C1167<br>$V_I = V_{CC}$ or GND         |                                       |                  | $\pm 1$ | $\mu$ A    |
| $r_i$     | Input resistance                                           | $V_{IC} = -7$ V to 7 V, Other input at 0 V | 4                                     | 17               |         | k $\Omega$ |
| $I_{CC}$  | Supply current (total package)                             | No load, Enabled                           | $V_I = V_{CC}$ or GND                 |                  | 4       | 6          |
|           |                                                            |                                            | $V_{IH} = 2.4$ V or 0.5 V, See Note 5 |                  | 5       | 9          |

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 8)**

| PARAMETER |                                                   | TEST CONDITIONS              | MIN | TYP <sup>†</sup> | MAX | UNIT |
|-----------|---------------------------------------------------|------------------------------|-----|------------------|-----|------|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | See Figure 5                 | 9   | 17               | 27  | ns   |
| $t_{PHL}$ | Propagation delay time, high- to low-level output |                              | 9   | 17               | 27  | ns   |
| $t_{TLH}$ | Transition time, low- to high-level output        | $V_{IC} = 0$ V, See Figure 5 |     | 4                | 9   | ns   |
| $t_{THL}$ | Transition time, high- to low-level output        |                              |     | 4                | 9   | ns   |
| $t_{PZH}$ | Output enable time to high level                  | $R_L = 1$ kW, See Figure 6   |     | 13               | 22  | ns   |
| $t_{PZL}$ | Output enable time to low level                   |                              |     | 13               | 22  | ns   |
| $t_{PHZ}$ | Output disable time from high level               |                              |     | 13               | 22  | ns   |
| $t_{PLZ}$ | Output disable time from low level                |                              |     | 13               | 22  | ns   |

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

NOTE 8: Measured per input while the other inputs are at  $V_{CC}$  or GND



## PARAMETER MEASUREMENT INFORMATION

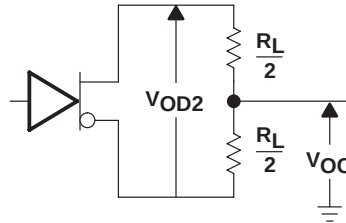
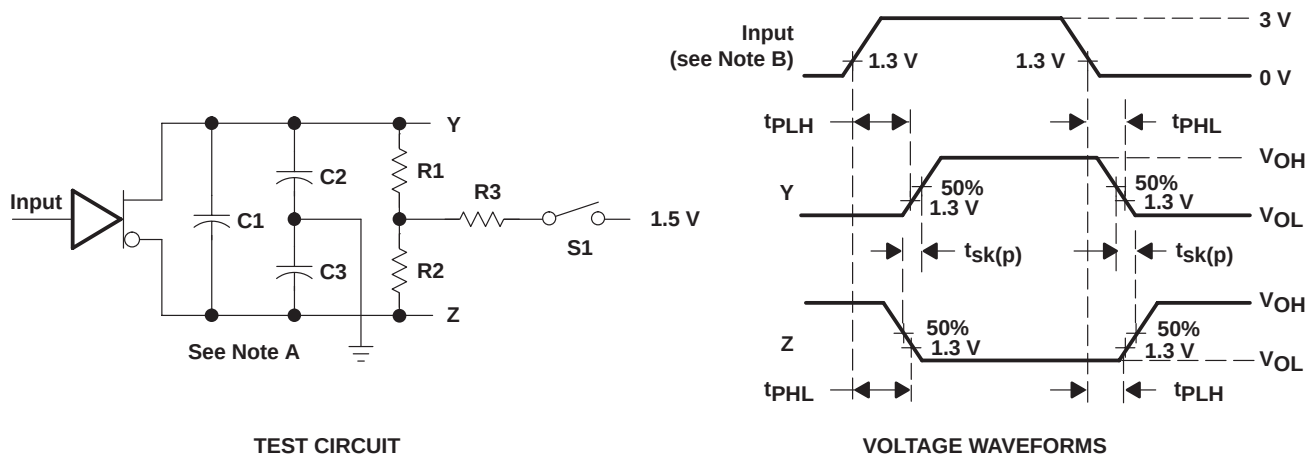
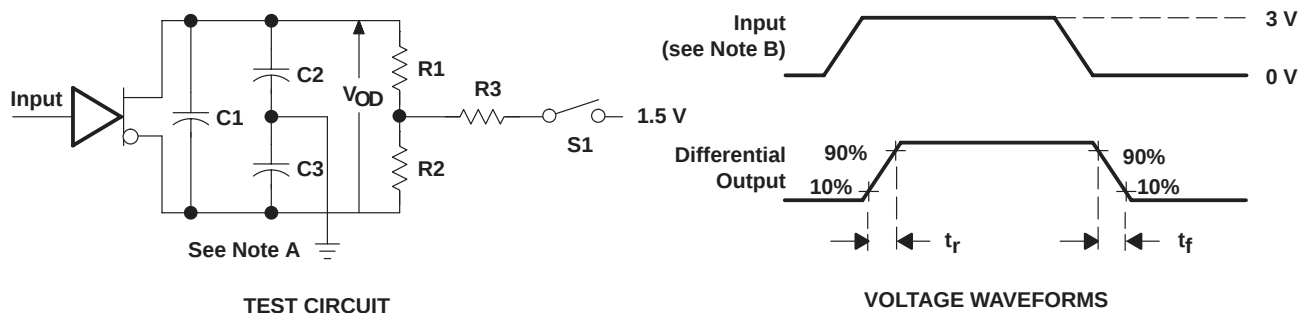


Figure 1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$



- NOTES: A. C1, C2, and C3 include probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r = t_f \leq 6$  ns.

Figure 2. Driver Test Circuit and Voltage Waveforms



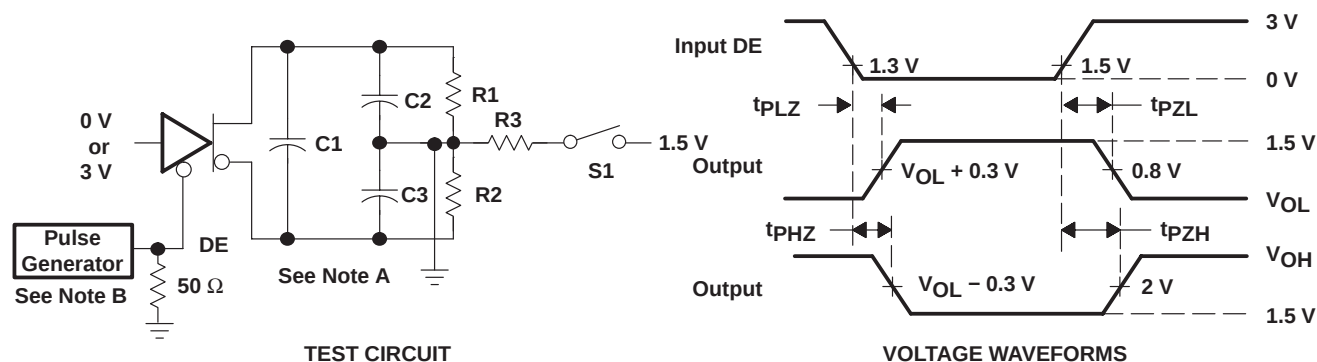
- NOTES: A. C1, C2, and C3 include probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r = t_f \leq 6$  ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

# SN65C1167, SN75C1167, SN65C1168, SN75C1168 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

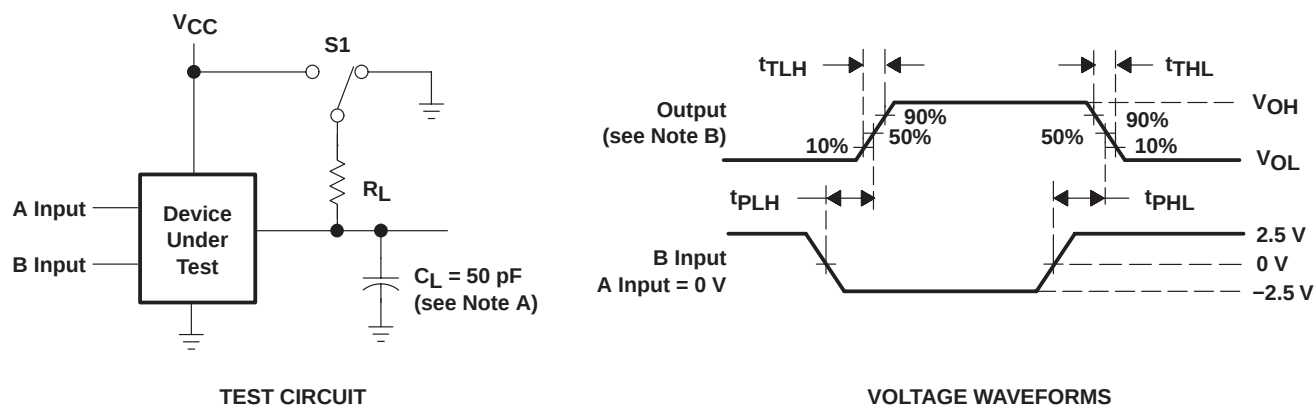
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## PARAMETER MEASUREMENT INFORMATION



NOTES: A. C1, C2, and C3 include probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r = t_f \leq 6$  ns.

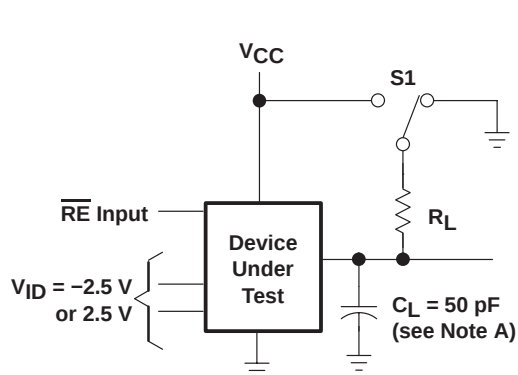
Figure 4. Driver Test Circuit and Voltage Waveforms



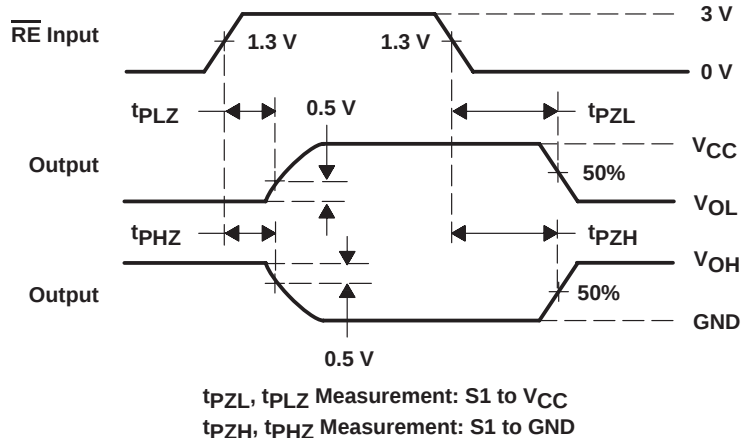
NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq 6$  ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r = t_f \leq 6 \text{ ns}$ .

Figure 6. Receiver Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN65C1167NSLE    | OBSOLETE              | SO           | NS              | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN65C1167NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1167NSRE4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN65C1168NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN65C1168NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168NSRG4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168PW      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168PWE4    | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168PWR     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65C1168PWRE4   | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1167DBR     | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1167DBRE4   | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1167N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75C1167NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75C1167NSLE    | OBSOLETE              | SO           | NS              | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN75C1167NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1167NSRG4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168DBR     | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168DBRE4   | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75C1168NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75C1168NSLE    | OBSOLETE              | SO           | NS              | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN75C1168NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168NSRE4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168NSRG4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75C1168PW      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168PWE4    | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168PWR     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75C1168PWRE4   | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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