UDIMM DDR4 2400 16GB Datasheet

(SQR-UD4N16G2K4HNHAC)

Features:

- **Compliance with**
  - JEDEC Standard 288-pin small-outline dual in-line memory module
  - Intend for PC4-19200 application
  - Backward compatible with PC4-17000 and PC4-14900
  - Bi-Directional Differential Data Strobe
  - 8 Bit pre-fetch, 16 Internal banks
  - Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
  - Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
  - On-Die Termination (ODT)
  - On-Board EEPROM
  - Internal Vref DQ level generation is available
  - RoHS and Halogen free
  - Golden connector

- **SDRAM Configuration:** SK Hynix DDR4 8Gb 1Gx8 SDRAM

- **Capacities**

  8GB 1Gbx64 1Rank

  16GB 2Gbx64 2 rank

- **Performance**
  - DDR4-2400 PC4-19200 CL17
  - DDR4-2133 PC4-17000 CL15
  - DDR4-1866 PC4-14900 CL13

- **DRAM Type**
  - DDR4 UDIMM

- **Temperature ranges**

Operating:

  - Standard: 0°C to 85°C

Storage:

  - -50°C to 100°C

- **Supply voltage**
  - V_{DD}=V_{DDQ}=1.2 Volt (TYP)
  - V_{PP}=2.5 Volt (TYP)
  - V_{DDSPD}=2.25V~3.6V
- **Operation Current**
  - Active mode(max):

    8GB:1.03A

    16GB:1.56 A

    (T_{CASE}: 0°C to 95°C)

- **Form factor**
  - DDR4 288pin UDIMM

- **Shock &Vibration**
  - Shock: 1000G@1ms
  - Vibration: 20 G

- **Certification and Compliance**
  - RoHS
  - REACH
  - CE
  - FCC

Revision History:

Rev.	Description	Date
0.1	Internal release	2017/07/20
0.2	Part Number Recode	2017/07/20
1.0	Official release	2017/07/20

CONTENTS

1. ADVANTECH Memory Product Description

1.1 Introduction

ADVANTECH Unbuffered DDR4 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered DIMMs are intended for use as main memory when installed in systems such as embedded systems and personal computers.

1.2 Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
	CL=13	CL=15	CL=17				
PC4-19200	1866	2133	2400	14.16	14.16	32	46.16

1.3 Ordering Information

DDR4 UDIMM					
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank
SQR-UD4N16G2K4HNHAC	16GB	PC4-19200	2Gx64	16	2

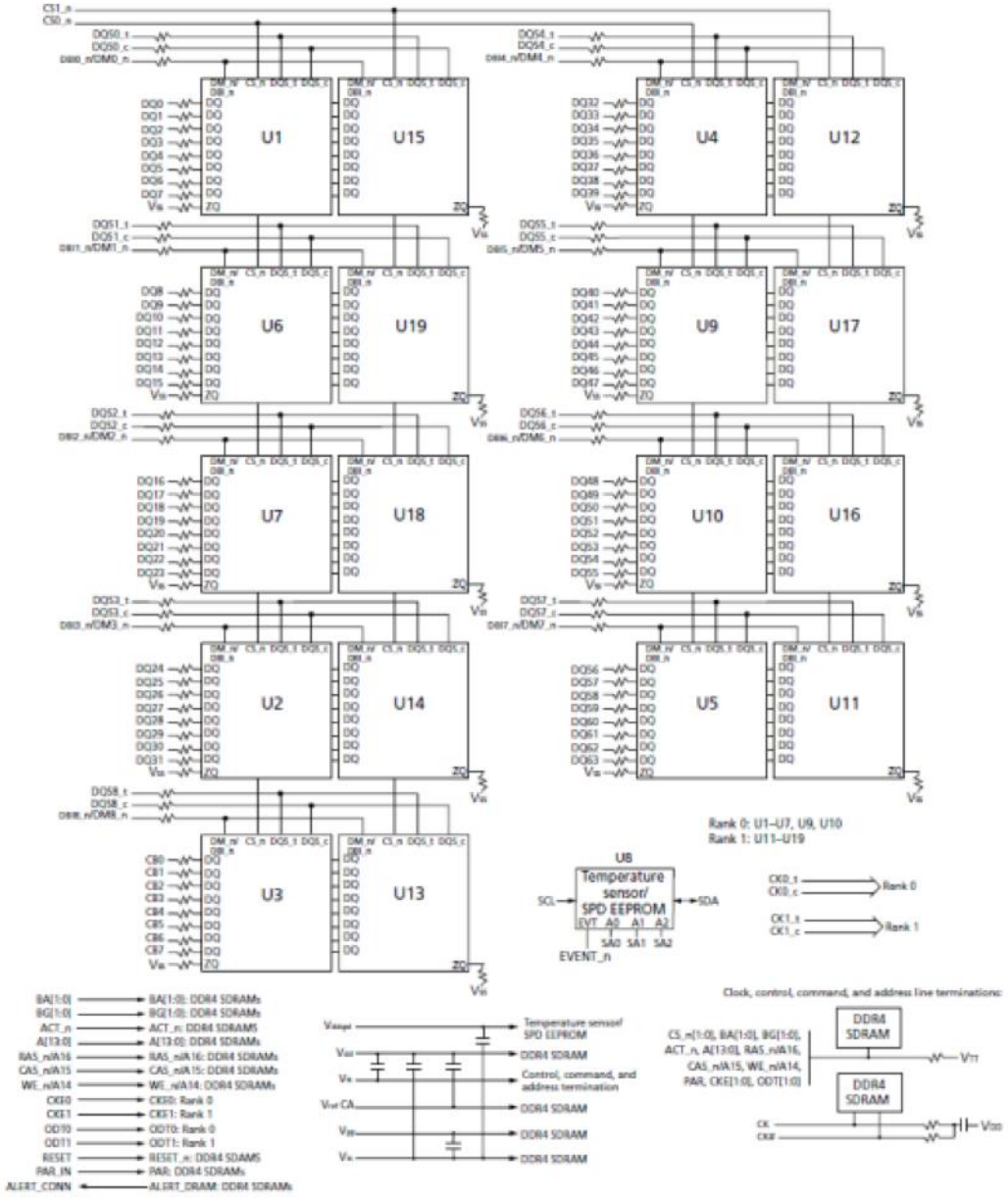
1.4 ADVANTECH Value Added Service

ADVANTECH DIMM provides specialized services to IPC designing customized hardware and systems by offering:

- Locked BOM control with customer product change notification(PCN)
- Pre-installed software, custom software imaging and ID strings
- Custom packaging and labeling
- Comprehensive supply-chain management
- Customer specified testing
- Localized Field Application Engineering for complete pre and post-sale technical support
- Optional Extend Temperature, ASTM B809-95 certified and conformal coating service.

2. ADVANTECH Memory Module Block Diagram

- DDR4 16GB, 1Gx8 base, 2Rank



Note:

- Unless otherwise noted, resistor value are 15Ω±5%
- ZQ resisters are 240Ω±1%. For all other resistor values refer to the appropriated wiring diagram
- To connector the SPDA2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The Value for R1 and R2 are not critical. Any value less than 100Ω may be used.

3. Environment Requirement

3.1.ADVANTECH DIMM Parameter

ADVANTECH DIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating& storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR4 DRAM component specification.
2. Up to 9850 ft.

3.2.SDARM parameter by device density

RTT_Nom Setting	Parameter		8Gb	Units
tREFI	Average periodic refresh interval	0°C≦T_{CASE}≦**85**°C	7.8	µs
		85°C≦T_{CASE}≦**95**°C	3.9	µs

4. Absolute Maximum Rating

4.1.Module Absolut Maximum Rating

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.5	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to +1.5	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to +1.5	V	1
V_{PP}	Voltage on VPP supply relative to Vss	-0.4 to +3.0	V	2

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.

4.2.SDRAM Absolut Maximum Rating

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	℃	1,2
		Extended Temp.(optional)	85 to 95	℃	1,3
T_{STG}	Storage Temperature		-55 to 150	℃	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater than0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

5. Pin Configurations (Front side/Back side)

5.1.DDR4 UDIMM Pin Assignment

Pin	I/O	Pin	I/O	Pin	I/O	Pin	I/O	Pin	I/O	Pin	I/O	Pin	I/O	Pin	I/O
1	NC	145	NC	37	VSS	181	DQ29	73	VDD	217	VDD	109	VSS	253	DQ41
2	VSS	146	VREFCA	38	DQ24	182	VSS	74	CK0_t	218	CK1_t	110	DM5_n/ DBI5_n,NC	254	VSS
3	DQ4	147	VSS	39	VSS	183	DQ25	75	CK0_c	219	CK1_c	111	NC	255	DQS5_c
4	VSS	148	DQ5	40	DM3_n/ DBI3_n,NC	184	VSS	76	VDD	220	VDD	112	VSS	256	DQS5_t
5	DQ0	149	VSS	41	NC	185	DQS3_c	77	VTT	221	VTT	113	DQ46	257	VSS
6	VSS	150	DQ1	42	VSS	186	DQS3_t	78	EVENT_n,NF	222	PARITY	114	VSS	258	DQ47
7	DM0_n_t/ DBI0_n	151	VSS	43	DQ30	187	VSS	79	A0	223	VDD	115	DQ42	259	VSS
8	NC	152	DQS0_c	44	VSS	188	DQ31	80	VDD	224	BA1	116	VSS	260	DQ43
9	VSS	153	DQS0_t	45	DQ26	189	VSS	81	BA0	225	A10/AP	117	DQ52	261	VSS
10	DQ6	154	VSS	46	VSS	190	DQ27	82	RAS_n /A16	226	VDD	118	VSS	262	DQ53
11	VSS	155	DQ7	47	CB4/NC	191	VSS	83	VDD	227	NC	119	DQ48	263	VSS
12	DQ2	156	VSS	48	VSS	192	CB5,NC	84	CS0_n	228	WE_n/ A14	120	VSS	264	DQ49
13	VSS	157	DQ3	49	CB0/NC	193	VSS	85	VDD	229	VDD	121	DM6_n/ DBI6_n	265	VSS
14	DQ12	158	VSS	50	VSS	194	CB1,NC	86	CAS_n/ A15	230	NC	122	NC	266	DQS6_c
15	VSS	159	DQ13	51	DM8_n/ DBI8_n,NC	195	VSS	87	ODT0	231	VDD	123	VSS	267	DQS6_t
16	DQ8	160	VSS	52	NC	196	DQS8_c	88	VDD	232	A13	124	DQ54	268	VSS
17	VSS	161	DQ9	53	VSS	197	DQS8_t	89	CS1_n	233	VDD	125	VSS	269	DQ55
18	DMI_n/ DBI1_n,NC	162	VSS	54	CB6 DBI8_n,NC	198	VSS	90	VDD	234	NC	126	DQ50	270	VSS
19	NC	163	DQS1_c	55	VSS	199	CB7,NC	91	ODT1	235	NC	127	VSS	271	DQ51
20	VSS	164	DQS1_t	56	CB2/NC	200	VSS	92	VDD	236	VDD	128	DQ60	272	VSS
21	DQ14	165	VSS	57	VSS	201	CB3,NC	93	NC	237	NC	129	VSS	273	DQ61
22	VSS	166	DQ15	58	RESET_n	202	VSS	94	VSS	238	SA2	130	DQ56	274	VSS
23	DQ10	167	VSS	59	VDD	203	CKE1	95	DQ36	239	VSS	131	VSS	275	DQ57
24	VSS	168	DQ11	60	CKE0	204	VDD	96	VSS	240	DQ37	132	DM7_n/ DBI7_n,NC	276	VSS
25	DQ20	169	VSS	61	VDD	205	NC	97	DQ32	241	VSS	133	NC	277	DQS7_c
26	VSS	170	DQ21	62	ACT_n	206	VDD	98	VSS	242	DQ33	134	VSS	278	DQS7_t
27	DQ16	171	VSS	63	BG0	207	BG1	99	DM4_n/ DBI4_n,NC	243	VSS	135	DQ62	279	VSS
28	VSS	172	DQ17	64	VDD	208	ALERT_n	100	NC	244	DQS4_c	136	VSS	280	DQ63
29	DM2_n/ DBI2_n,NC	173	VSS	65	A12/BC_n	209	VDD	101	VSS	245	DQS4_t	137	DQ58	281	VSS
30	NC	174	DQS2_c	66	A9	210	A11	102	DQ38	246	VSS	138	VSS	282	DQ59
31	VSS	175	DQS2_t	67	VDD	211	A7	103	VSS	247	DQ39	139	SA0	283	VSS
32	DQ22	176	VSS	68	A8	212	VDD	104	DQ34	248	VSS	140	SA1	284	VSSSPD
33	VSS	177	DQ23	69	A6	213	A5	105	VSS	249	DQ35	141	SCL	285	SDA
34	DQ18	178	VSS	70	VDD	214	A4	106	DQ44	250	VSS	142	VPP	286	VPP
35	VSS	179	DQ19	71	A3	215	VDD	107	VSS	251	DQ45	143	VPP	287	VPP
36	DQ28	180	VSS	72	A1	216	A2	108	DQ40	252	VSS	144	NC	288	VPP

Not+B12:Q39e:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

5.2.Pin Description

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0-SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CEK1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0-CB7	DIMM ECC check bits		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

6. ADVANTECH SDRAM Operation Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
I_{VTT}	Termination reference voltage (DC) –command/address bus	-750	-	750	mA	
V_{TT}	Termination Voltage	0.49 × VDD - 20mV	0.5 × VDD	0.51 × VDD + 20mV	V	4
I_I	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	-2.0	-	2.0	µA	5
II/O	DQ leakage; 0V < Vin < VDD	-4.0	-	4.0	µA	5
I_{OZpd}	Output leakage current; VOUT = VDD; DQ is disabled	-	-	5.0	µA	5,6
I_{OZpu}	Output leakage current; VOUT =VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	V_{REF} + 0.125	-	V_{DDQ} + 0.3	µA	1
I_{OZpd}	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)	-2.0	-	2.0	µA	5

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

7. Operating, Standby and Refresh Currents

- **16GB UDIMM**(2Rank 1Gx8 DDR4 SDRAMs)

- Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	470	63	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	505	63	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stablest 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	575	63	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	603	63	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	325	54	mA

IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	395	54	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	350	54	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	305	54	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	350	54	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	305	54	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	350	54	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	205	54	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	315	54	mA

IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	450	54	mA
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	495	54	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: s Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	295	54	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1100	54	mA
IDD4RA	Operating Burst Read Current (AL=CL-1)	1135	54	mA

	AL = CL-1, Other conditions: see IDD4R			
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	1125	54	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	900	54	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	945	54	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	900	54	mA
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	830	54	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	945	54	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1565	189	mA

IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1315	162	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1035	126	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	225	72	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	295	72	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	170	54	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	225	72	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1035	95	mA
IDD8	Maximum Power Down Current TBD	145	36	mA

8. Serial Presence Detect

- SQR-UD4N16G2K4HNHAC

Byte	Description	Function support	Byte Value (Hexadecimal)
0	SPD BYTES USE/TOTAL BYTES AVAILABLE/CRC COVERAGE	SPD Bytes Used : 384 / SPD Bytes Total : 512	23
1	SPD REVISION	Rev 1.1	11
2	DRAM DEVICE TYPE	DDR4 SDRAM	0C
3	MODULE TYPE (FORM FACTOR)	nECC UDIMM	02
4	SDRAM DEVICE DENSITY BANKS	4BG/4BK/8Gb	85
5	SDRAM DEVICE ADDRESSING	16/10	21
6	SDRAM DEVICE TYPE (ARCHITECURE)	SDP	00
7	SDRAM DEVICE OPTIONAL FEATURES	Unlimited MAC	08
8	SDRAM DEVICE THERMAL REFRESH OPTIONS	Reserved	00
9	OTHER SDRAM OPTIONAL FEATURES	hPPR, sPPR supported	60
10	SECONDARY SDRAM PACKAGE TYPE	Blank	00
11	NOMINAL MODULE VOLTAGE (VDD)	1.2V	03
12	MODULE ORG. (PACKAGE RANKS DEVICE WIDTH)	2Rx8	09
13	MODULE MEMORY BUS WIDTH	LP/x64	03
14	MODULE THERMAL SENSOR SUPPORT	Thermal sensor supported	80
15	EXTENDED MODULE TYPE	Blank	00
16	BYTE 16 RESERVED	Blank	00
17	TIMEBASES (MTB FTB)	MTB : 125ps, FTB : 1ps	00
18	SDRAM DEVICE TCKMIN	0.833ns	07
19	SDRM DEVICE TCKMAX	1.6ns	0D
20	CL7 THROUGH CL14 SUPPORT	14, 13, 12, 11, 10	F8
21	CL15 THROUGH CL22 SUPPORT	18, 17, 16, 15	0F
22	CL23 THROUGH CL30 SUPPORT		00
23	CL31 THROUGH CL36 SUPPORT-CL RNG		00

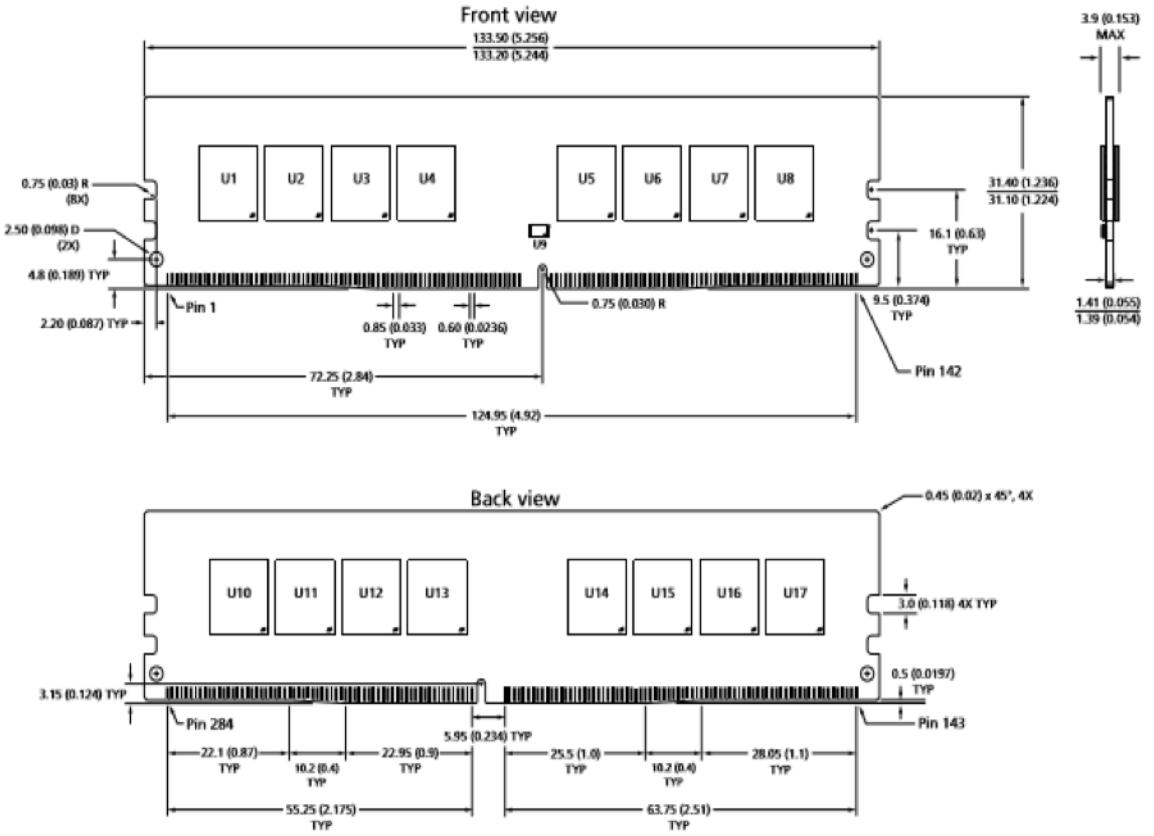
24	MIN CAS LATENCY (TAAMIN)	13.75ns	6E
25	MIN RAS TO CAS DELAY (TRCDMIN)	13.75ns	6E
26	MIN ROW PRECHARGE DELAY (TRPMIN)	13.75ns	6E
27	UPPER NIBBLE TRASMIN, TRCMIN	32ns / 45.75ns	11
28	MIN ACTIVE TO PRECHARGE DELAY (TRASMIN) LSB	32ns	00
29	MIN ACTIVE TO ACTIVE/REFRESH DELAY (TRCMIN) LSB	45.75ns	6E
30	MIN REFRESH RECOVERY DELAY (TRFC1MIN) LSB	350ns	F0
31	MIN REFRESH RECOVERY DELAY (TRFC1MIN) MSB	350ns	0A
32	MIN REFRESH RECOVERY TIME DELAY (TRFC2MIN) LSB	260ns	20
33	MIN REFRESH RECOVERY DELAY (TRFC2MIN) MSB	260ns	08
34	DDR4-MIN REFRESH RECOVERY DELAY (TRFC4MIN) LSB	160ns	00
35	MIN REFRESH RECOVERY DELAY (TRFC4MIN) MSB	160ns	05
36	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) UPPER NIB	21ns	00
37	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) LSB	21ns	A8
38	MIN ACTIVE TO ACTIVE DELAY (TRRD_SMIN) DIFRNT BANK GRP	3.3ns	1B
39	MIN ACTIVE TO ACTIVE DELAY (TRRD_LMIN) SAME BANK GRP	4.90ns	28
40	MIN CAS TO CAS DELAY, SAME BG (TCCDLMIN)	5.0ns	28
41	TWRMIN MSB	15ns	00
42	TWRMIN LSB	15ns	78
43	TWTR_LMIN/TWTR_SMIN - MSB (UPPER NIBLS)	2.5ns/7.5ns	00
44	TWTR_SMIN - LSB	2.5ns	14
45	TWTR_LMIN - LSB	7.5ns	3C
46-59	RESERVED BYTES 46 - 59	Blank	00
60	DDR4-BIT MAP, DQ0 - 3	DQ0-3	15
61	DDR4-BIT MAP, DQ4 -7	DQ4-7	2B
62	DDR4-BIT MAP, DQ8 - 11	DQ8-11	16

63	DDR4-BIT MAP, DQ12 - 15	DQ12-15	36
64	DDR4-BIT MAP, DQ16 - 19	DQ16-19	0B
65	DDR4-BIT MAP, DQ20 - 23	DQ20-23	2B
66	DDR4-BIT MAP, DQ24 - 27	DQ24-27	0C
67	DDR4-BIT MAP, DQ28 - 31	DQ28-31	36
68	DDR4-BIT MAP, CB0 - 3	CB0-3	00
69	DDR4-BIT MAP, CB4 - 7	CB4-7	00
70	DDR4-BIT MAP, DQ32 - 35	DQ32-35	36
71	DDR4-BIT MAP, DQ36 - 39	DQ36-39	15
72	DDR4-BIT MAP, DQ40 - 43	DQ40-43	2B
73	DDR4-BIT MAP, DQ44 - 47	DQ44-47	0C
74	DDR4-BIT MAP, DQ48 - 51	DQ48-51	2C
75	DDR4-BIT MAP, DQ52 - 55	DQ52-55	16
76	DDR4-BIT MAP, DQ56 - 59	DQ56-59	2B
77	DDR4-BIT MAP, DQ60 - 63	DQ60-63	0C
78-116	RESERVE BYTES 78 - 116	Blank	00
117	FTB OFFSET - TCCDLMIN	5.0ns	00
118	FTB OFFSET - TRRD_LMIN	4.90ns	9C
119	FTB OFFSET - TRRD_SMIN	3.3ns	B5
120	FTB OFFSET - TRCMIN	46.75ns	00
121	FTB OFFSET - TRPMIN	13.75ns	00
122	FTB OFFSET - TRCDMIN	13.75ns	00
123	FTB OFFSET - TAAMIN	13.75ns	00
124	FTB OFFSET - TCKMAX	1.6ns	E7
125	FTB OFFSET - TCKMIN	0.833ns	D6
126-127	CRC FOR BYTES 0 - 125, BASE CONFIG	CRC cover 0~125 byte	DF 5C
128	RAW CARD EXT. AND MODULE NOM. HEIGHT	31.25	11
129	MODULE MAX THICKNESS	1.2/1.2	11
130	RAW CARD ID	B1	21

131	UDIMM ADDRESS MAPPING - RDIMM MODULE ATTRIBUTES	Mirrored	01
132	RDIMM HEAT SPREADER SOLUTION	Blank	00
133	RDIMM REGISER MFR. ID (LSB)	Blank	00
134	REGISTER MFR. ID (MSB)	Blank	00
135	REGISTER REVISION NUMBER	Blank	00
136	REGISTER ADDRESS MAPPING	Blank	00
137	REG OUTPUT DRIVE FOR CONTROL	Blank	00
138	REG OUTPUT DRIVE FOR CLOCK	Blank	00
139-253	RESERVE BYTES 139 - 253	Blank	00
254-255	CRC FOR MODULE SPECIFIC BYTES 128-253	CRC cover 128~253 byte	74 DF
256-319	BYTES 256 - 319 RESERVED	Blank	00
320	MODULE MFR. ID CODE (LSB)		00
321	MODULE MFR. ID COD (MSB)		00
322	MODULE MFR. LOCATION	Taiwan	02
323-324	MODULE MFR. DATE	-	-
325-328	MODULE SERIAL NUMBER		00
329-348	MODULE PART NUMBER	SQR-UD4N16G2K4HNHAC	53 51 52 2D 55 44 34 4E 31 36 47 32 4B 34 48 4E 48 41 43 20
349	MODULE PCB REV		00
350	DRAM MFR. ID CODE (LSB)	SK hynix	80
351	DRAM MFR. ID CODE (MSB)	SK hynix	AD
352	DEVICE DIE REV (PART MARKING)	Undefined	FF
353-383	BYTES 353 - 383 RESERVED		-
384-511	BYTES 384-511 END USER RESERVED	Blank	00

9. Package Dimension

-16GB DDR4 UDIMM, 2Gx64, 2 Rank



Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

10. Reliability Specifications

10.1. Environmental Conditions

Environmental specifications are following MIL-STD-810F, as below table.

Environment	Specification
Storage Temperature	-50°C ~ +100°C
Operating Temperature	0°C to 85°C (Standard);
Vibration	20G
Shock	1000G@1ms